Amendments to the Drawings:

The attached sheet of drawings includes changes to Fig. 18. This sheet, which includes Figs. 18 and 18a, replaces the original sheet including Fig. 18 and 18a.

Attachment: Replacement Sheet

Annotated Sheet Showing Changes

REMARKS/ARGUMENTS

Claims 1-29 are pending. Claims 4 and 10 are amended.

FIG. 18 is objected to. FIG. 18 is amended, as suggested by the Examiner. Therefore, it is respectfully requested that the above objection be withdrawn.

Claim 10 is objected to because of informalities. Claim 10 is amended to correct a typographical error. Accordingly, it is respectfully requested that the above objection be withdrawn.

Claim 4 is objected to because "two counts should be present." Claim 4 is amended to incorporate Examiner's suggestion. Accordingly, it is respectfully requested that the above objection be withdrawn.

Claims 18-29 are allowed. Claims 4, 6-10 and 12-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 1-3, 5 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Kao (US 4,815,109). Applicant submits that all of the claims currently pending in this application are patentably distinguishable over the cited references, and reconsideration and allowance of this application are respectfully requested.

Independent claim 1 recites "generating a clock error signal as a function of one or more data control flags; and fractionally resampling the data as a function of the clock error signal." Kao does not disclose the above limitations.

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First, Kao does not disclose "generating a clock error signal as a function of one or more <u>data control flags</u>." Applicants respectfully disagree with the statement in the Office action that the Derived CLKA of Kao is a control flag. Kao is clear that Derived CLKA is a clock, not a control flag. For example, referring to FIG. 1 Kao explains that "[o]n the receiving end of the data communications medium 20 a similar DCE 22 is provided which receives the transmission from DCE 18 and derives <u>clock signal CLKA</u> from the transmitted data. <u>This clock signal CLKA</u> is delivered to a phase locked loop frequency synthesizer 24 which uses known techniques for synthesizing signal CLK1 from the <u>derived clock signal CLKA</u>." (Col. 1, lines 42-49, underlining added.).

Furthermore, referring to FIG. 2 Kao explains that "[o]n the received side however, the <u>derived CLKA is provided</u> to a slip detector 50 as well as to an intelligent expander 52. <u>A second clock 54 is also provided</u> which produces a local 8 Khz signal which is used to clock the digital to analog converter 28. . . . Slip detector 50 produces a signal SLIP which indicates that a one cycle slip has occurred between the <u>derived clock A</u> (CLKA) and signal CLK2. (Col. 3, line 57 to col. 4, line 1, underlining added.). Therefore, Derived CLKA of Kao is a clock signal and NOT a data flag.

Second Kao does not fractionally resamples the data. Rather, expander 52 of Kao uses a signal SLIP (alleged "error signal") to "throw away" ("discard") or "repeat" ("add") a sample of the signal, rather than "resample" the data. (Col. 4, lines 7-19, and Abstract.). In fact, the sampling rate of Kao

is provided by the A/D 12 (FIGs. 1 and 2) and remains constant through out the process.

In contrast, the claimed invention resamples the data. For example, as described with respect to FIG. 17B, "it is assumed that the input sample count, shown as samples 1, 2, 3, and 4, is 65537 and the output sample count, shown as samples A, B, C and D, is 65536 thereby creating a slight overflow condition. The distance between for example, sample 2 and B is equal to 1/65536 of one input sample period. Therefore, an incoming 8 kHz signal would have to be <u>resampled at the rate of (65536)(8 kHz) or 524.288 MHz to generate the additional samples</u> required to eliminate the overflow condition. Referring to FIG. 17C, in the extreme 65535 zeros would be placed between each individual data sample of the input signal stored in a data buffer. In a typical application <u>eighteen data points would be used to compute the resampling</u>. The number of data points represents a trade between the quality of the conversion and computational complexity. Low pass filter coefficients (Coef-1 through Coef-1179648) would be computed which, when applied to the samples stored in the buffer yield the resampled signal." (Page 50, line 27 to page 51, line 8, underlining added.). Consequently, claim 1 is not anticipated by Kao.

Independent claim 11 includes, among other limitations, "wherein the sample tracker <u>fractionally resamples</u> the sampled data as a function of the clock error signal." As explained above, the system of Kao does not resample the data. Rather, it "throws away" ("discards") or "repeats" ("adds") a sample of the signal. Therefore, claim 11 is not anticipated by Kao either.

In short, the independent claims 1 and 11 define a novel and unobvious invention over the cited references. Remaining dependent claims 2-10 and 12-17 are dependent from independent claims 1 and 11, respectively and include all the limitations of their respective independent claims and additional limitations therein. Accordingly, these claims are also allowable over the cited references, as being dependent from allowable independent claims and for the additional limitations they include therein.

In view of the foregoing amendments and remarks, it is respectfully submitted that this application is now in condition for allowance, and accordingly, reconsideration and allowance are respectfully requested.

Respectfully submitted,

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RRT/clv
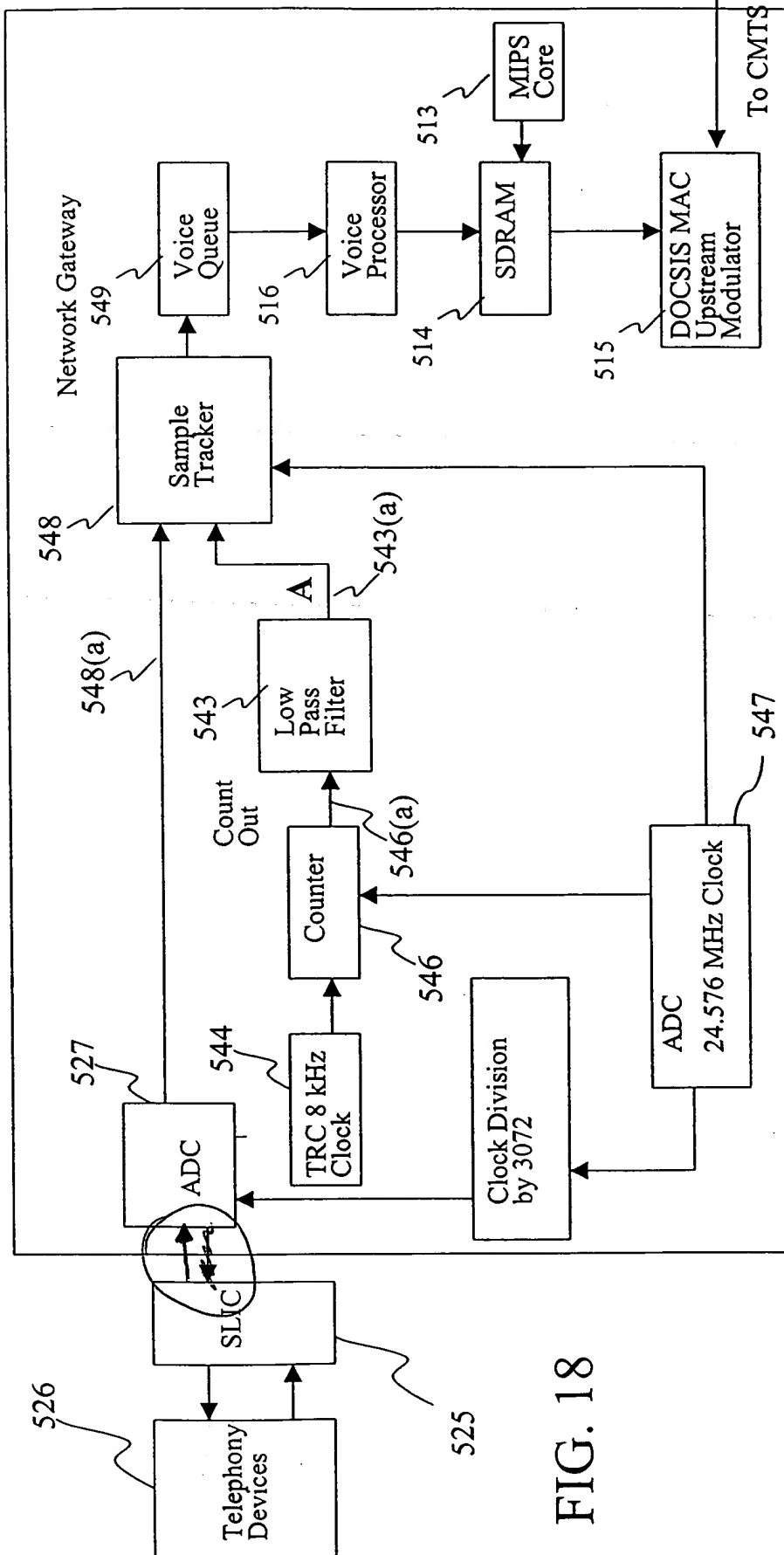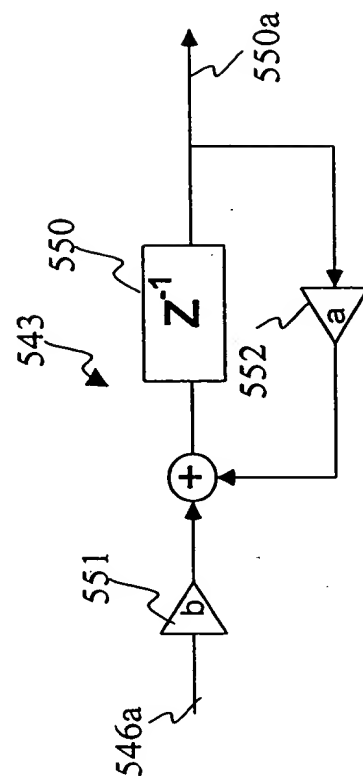CLV PAS613429.1-*-03/17/05 9:39 AM

FIG. 18A

FIG. 18